

REMARKS

Claims 1-11 have been examined on their merits.

The Patent Office objects to claims 2, 3, 5-8, 10 and 11 as being dependent upon a rejected base claim. Applicants thank the Patent Office for indicating that claims 2, 3, 5-8, 10 and 11 would be allowed if rewritten in independent form. However, instead of rewriting claims 2, 3, 5-8, 10 and 11 in independent form, Applicants respectfully traverse the prior art rejections for the reasons set forth below.

Applicant herein amends claims 1, 4 and 9 to clarify that only one of the first and second digital signals is delayed by a period equal to an integer multiple of the sampling period.

Claims 1-11 are all the claims presently pending in the application.

2. Claims 1 and 4 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Meehan (U.S. Patent No. 6,115,419). Applicants traverse the rejection of claims 1, 4 and 9 for at least the reasons discussed below.

Meehan fails to teach or suggest at least delaying, in a digital manner, either a first digital signal or a second digital signal by a period equal to an integer multiple of the sampling period of the first and second digital signals, as recited in claim 1. The Patent Office allege that one of the two digital signals is delayed by passing through “phase shifter (230) and a second feed-forward equalizer (232) with inherent multiple delay taps based on the sampling period.” *See* June 28, 2005 Office Action, page 4. The Patent Office further cites col. 4, lines 26-32 as support for its allegation.

Col. 4, lines 26-32 of Meehan states:

First $\pi/2$ phase shift circuit 230 is connected to second feedforward equalizer circuit 232. First $\pi/2$ phase shift circuit 230 shifts by 90 degrees the digital baseband signal at the input of second feedforward equalizer 232 with respect to the baseband signal at the input of first feedforward equalizer 228.

However, col. 4, lines 32-39 of Meehan states:

Under control of decision device 330, first feedforward equalizer circuit 228 modifies the input signal to form a beam in the direction of the desired signal and to form a null in the direction of the interfering signal. Similarly, under control of decision device 330, second feedforward equalizer circuit 232 modifies the $\pi/2$ phase shifted input signal to form a beam in the direction of the desired signal and to form a null in the direction of the interfering signal.

Meehan discloses that both a first digital signal and a second digital signal are delayed, since Figure 1 shows the identical circuitry (*i.e.*, $\pi/2$ phase shift circuit 252 is connected to second feedforward equalizer circuit 254) used for the second digital signal. In contrast, amended claim 1 now recites that only one of the first or second digital signals is delayed by an integer multiple of a sampling period, but not both the first and second digital signals. Thus, Applicants submit that claim 1 is allowable over Meehan, and respectfully request withdrawal of the § 102(e) rejection of claim 1.

With respect to claim 4, Applicants submit that claim 4 is allowable for at least reasons analogous to those discussed above with respect to claim 1. Applicants submit that claim 4 is allowable, and respectfully request that the Patent Office withdraw the § 102(e) rejection of claim 4.

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With respect to claim 9, Applicants submit that claim 9 is allowable for at least reasons analogous to those discussed above with respect to claim 1. Applicants submit that claim 9 is allowable, and respectfully request that the Patent Office withdraw the § 102(e) rejection of claim 9.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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